UNITED STATES PATENT APPLICATION

for

A SLEW RATE CONTROL MECHANISM

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A SLEW RATE CONTROL MECHANISM

FIELD OF THE INVENTION

[0001] The present invention relates to computer systems; more particularly, the present invention relates to high speed busses within computer systems.

BACKGROUND

[0002] In the past there has not been much concern with regards to maintaining signal edge rates (or slew rates) on busses. This is because there were little negative effects of having variable slew rates on slower speed busses. However as bus speeds increase, there are tighter restrictions on edge rates [volts/nanoseconds] of a signal switching high to low, or vice versa. If the slew rate is faster or slower, there could potentially be problems with signal integrity and transmissions. Thus, there are tight timing windows for signal transitions on the current high-speed busses.

[0003] Currently, the hardware design for integrated circuits are manually simulated and are deduced from a mechanism indicating process voltage and temperature (PVT) to determine the slew rate of the signals being transmitted on a high-speed bus. However if a mechanism indicating (PVT) is malfunctioning, it is impossible to determine slew rate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The present invention will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the invention. The drawings, however, should not be taken to limit the invention to the specific embodiments, but are for explanation and understanding only.

[0005] **Figure 1** illustrates one embodiment of a computer system;

[0006] **Figure 2** illustrates a block diagram of one embodiment of a memory control hub;

[0007] **Figure 3** illustrates embodiment of a slew rate detection circuit; and

[0008] **Figure 4** illustrates one embodiment of a reference current generator.

DETAILED DESCRIPTION

[0009] A slew rate control mechanism is described. In the following description, numerous details are set forth. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring the present invention.

[0010] Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

[0011] **Figure 1** is a block diagram of one embodiment of a computer system 100. Computer system 100 includes a central processing unit (CPU) 102 coupled to bus 105. In one embodiment, CPU 102 is a processor in the Pentium® family of processors including the Pentium® II processor family, Pentium® III processors, and Pentium® IV processors available from Intel Corporation of Santa Clara, California. Alternatively, other CPUs may be used.

[0012] A chipset 107 is also coupled to bus 105. Chipset 107 includes a memory control hub (MCH) 110. MCH 110 may include a memory controller 112 that is coupled to a main system memory 115 via a memory bus. Main

system memory 115 stores data and sequences of instructions and code represented by data signals that may be executed by CPU 102 or any other device included in system 100.

[0013] In one embodiment, main system memory 115 includes dynamic random access memory (DRAM); however, main system memory 115 may be implemented using other memory types. Additional devices may also be coupled to bus 105, such as multiple CPUs and/or multiple system memories.

[0014] In one embodiment, MCH 110 is coupled to an input/output control hub (ICH) 140 via a hub interface. ICH 140 provides an interface to input/output (I/O) devices within computer system 100. For instance, ICH 140 may be coupled to a Peripheral Component Interconnect bus adhering to a Specification Revision 2.1 bus developed by the PCI Special Interest Group of Portland, Oregon.

[0015] According to one embodiment, the memory bus coupling MCH 110 and main memory 115 is a high-speed memory bus. **Figure 2** illustrates a block diagram of one embodiment of MCH 110 coupled to the memory bus. Although the attached bus is discussed herein as a memory bus, one of ordinary skill in the art will appreciate that other busses may be implemented without departing from the scope of the invention.

[0016] MCH 110 includes control logic 210, input/output (I/O) buffer 220 and slew rate detection circuit 230. Control logic 210 compensates the slew rate of a bus coupled to MCH. Particularly, control logic 210 examines slew rate

(SLEW) signals received from slew rate detection mechanism 230 and modifies the I/O buffer 220 slew rate based on the state of the examined signal. For instance, if the SLEW signal received from slew rate detection circuit 230 indicates that the slew rate is too fast, control logic 210 reduces the slew rate at I/O buffer 220. Similarly, if the SLEW signal received from slew rate detection circuit 230 indicates that the slew rate is too slow, the slew rate at I/O buffer 220 is increased.

[0017] I/O buffer 220 is coupled to control logic 220 and an I/O pad. I/O buffer 220 is implemented to transmit output signals from MCH, and receive input signals from the coupled bus. I/O buffer 220 drives signals with a specific impedance and slew rate onto the bus. In one embodiment, the slew rate of the signal is controlled by control logic 210.

[0018] Slew rate detection circuit 230 is coupled to control logic 210 and a second I/O pad. Slew rate detection circuit 230 detects the slew rate of the signal transmitted by I/O buffer 220 and determines whether the slew rate is too fast or too slow. In response, detection circuit 230 generates the SLEW signal that is transmitted to control logic 210. **Figure 3** illustrates one embodiment of slew rate detection circuit 230.

[0019] Referring to **Figure 3**, detection circuit 230 includes a capacitor C1 that is used integrate a waveform, which is to have its slew rate [dv/dt] adjusted. The resultant current C1*[dv/dt] is amplified and then compared to an internally generated reference current. This reference current Iref is proportional to the

integrator capacitance C1.

[0020] However, the currents are first converted to voltages. Thus, detection circuit 230 includes current-voltage converters 320 and 330. Converter 320 converts the received current to an associated voltage value. Converter 320 includes a transistor M2 that is configured as a diode connected device. This helps to maintain a constant voltage on the other end of the capacitance. Therefore, the signal current (Isr) in the capacitance is truly proportional to the rate of change of voltage with respect to time [dv/dt] on the I/O pad.

[0021] Similarly, converter 330 converts a reference current (Iref) to a reference voltage. The reference current is generated from a reference current generator 340. In one embodiment, reference current generator 340 is a switched capacitor circuit. **Figure 4** illustrates one embodiment of a reference current generator 340. Current generator 340 generates the reference current Iref at the drain of a transistor M3.

[0022] Current generator 340 also includes a capacitor C2 and transistors phi1 and phi2. The gates of transistors phi1 and phi2 receive non-overlapping clock signals. In one embodiment, the clocks have a frequency of 1/T. In one embodiment, the capacitor C2 has a capacitance equivalent to the capacitor C1 coupled to the I/O pad. Therefore, C1 = C2. In addition, reference current generator 340 receives a voltage Vdd.

[0023] As a result, Iref can be expressed as Vdd*C/[2*T]. Since Vdd and T can be maintained constant over process, voltage and temperature, the absolute

value of Iref is dependant on the capacitance of C2. Due to their dependence on the capacitance value, Isr and Iref track each other in spite of any process variations and minimize the total compensation error. In one embodiment, slew rate controllability from 0.5v/ns to 3v/ns can be achieved using this circuit implementation.

[0024] Referring back to **Figure 3**, the two currents Isr and Iref are compared at comparator 350 after being converted to voltages Vsr and Vref, respectively. In one embodiment, comparator 350 is an amplifier, as shown in **Figure 3**. However, other types of comparators may be implemented in other embodiments. If the Vsr value falls below Vref, the SLEW signal is transmitted to control logic 210 indicating that the slew rate is too slow. However, if the Vsr value is above Vref, the SLEW signal is transmitted to control logic 210 indicating that the slew rate is too fast.

[0025] The above-described slew rate control mechanism enables the slew rate to be controlled on high-speed I/O busses.

[0026] Whereas many alterations and modifications of the present invention will no doubt become apparent to a person of ordinary skill in the art after having read the foregoing description, it is to be understood that any particular embodiment shown and described by way of illustration is in no way intended to be considered limiting. Therefore, references to details of various embodiments are not intended to limit the scope of the claims which in themselves recite only those features regarded as the invention.